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In the specification:

Please substitute the following paragraphs in the specification for the specification as originally filed or most recently amended.

(Page 9, lines 4+):

Referring now to the drawings, and more particularly to Figure 1, there is shown, in cross-section, an exemplary pair of complementary NMOS and Pmos-PMOS transistors such as might comprise a CMOS pair in a portion of an integrated circuit. These transistors have been completed through the formation of silicide on the source, drain and gate regions to reduce resistance of contacts to be later applied thereto. The method of formation of these transistors and the particulars of their structures are unimportant to an understanding of the invention or its successful practice. It should be understood that while Figure 1 illustrates transistors prior to the application of the invention thereto, the illustration is intended to be highly schematic for clarity and no portion of Figure 1 is admitted to be prior art as to the invention.

(Page 9, lines 34+):

The transistors are otherwise of similar construction; each having a gate dielectric 20, a gate electrode 22, a sidewall spacer structure 24, 26 and source, drain and gate silicide regions 28, as will be familiar to those skilled in the art. Source and drain implant regions and extension and/or halo implant regions may be included as may be desired, as is well-known in the art.